VLSI ReVisited: from Analog to Digital

3-July-2023 to 28-July-2023

EXECUTIVE SUMMARY

IIIT Delhi and IEEE CASS-CSS Delhi Chapter present 4-weeks Online Summer School on VLSI for Employability Enhancement for Faculty, recent graduates working in industry, and graduating students. Facilitated by stellar faculty with decades of teaching and industry work experience, this refresher program includes 100 fast-paced contact hours including theory and lab sessions. The program has been highly acclaimed in the previous runs as a perfect launchpad for a successful career in VLSI Circuits and System Design.

Jointly Organized by

IIIT Delhi and IEEE Circuits and Systems Society-Control Systems Society (IEEE CASS-CSS), Delhi chapter under the aegis of Chip to Startup Program of Ministry of Electronics and IT (MeitY), Govt of India

About IIIT Delhi

Indraprastha Institute of Information Technology, Delhi (IIIT-Delhi or IIIT-D) was created as a State University by an act of Delhi Government (The IIIT Delhi Act, 2007) empowering it to do research and development, and grant degrees. Established in 2008, the institute has grown to be recognized as one of the most promising young institutions for education and research in India.

In a relatively short time, it has earned an excellent reputation in India and abroad for being a centre of quality education and research in IT and interdisciplinary areas. It has highly qualified faculty that pursues bleeding edge collaborative research and publishes in the top venues worldwide. It is ranked #4 among all universities in India in the Times Higher Education world university rankings 2021 and #4 among all technical schools in India in the Dataquest T-School rankings 2021. The Institute was awarded 'Excellence in Faculty' in the 7th Higher Education Excellence Awards 2021 by the Federation of Indian Chambers of Commerce & Industry (FICCI).

About iHub Anubhuti

iHub Anubhuti is a Technology Innovation Hub (TiH) on "Cognitive Computing and Social Sensing" for Interdisciplinary Cyber-Physical Systems (ICPS) as a Section 8 Company(incorporated by IIIT Delhi) under the aegis of the National Mission on Interdisciplinary Cyber-Physical Systems (NM-ICPS) of the Department of Science and Technology, Government of India.

iHub Anubhuti aims at building collaboration between industries, academia, and government agencies on developing data-driven cognitive computing solutions. It also encourages and promotes entrepreneurial activities and start-ups emanating from the projects in the areas of Machine Learning, Artificial Intelligence, Cognitive Computing & Social Sensing

About IEEE, CAS Society, and CS Society

IEEE is the world's largest technical professional organization dedicated to advancing technology for the benefit of humanity. Its highly cited publications, conferences, technology standards, and professional and educational activities. IEEE is the trusted "voice" for engineering, computing, and technology information around the globe.

The IEEE Circuits and Systems (CAS) Society is the leading organization that promotes the advancement of the theory, analysis, computer-aided design and practical implementation of circuits, and the application of circuit theoretic techniques to systems and signal processing.

The Control Systems (CS) Society is dedicated to the advancement of the theory and practice of systems and control with focus on promoting scientific, technological, and educational advancements in the fields of automatic control, decision making, theory and applications, all over the world.

About Faculty of the Program

Dr. Anuj Grover pursued B.Tech in Electrical Engineering from IIT Delhi, MS in Electronic Circuits and Systems from University of California, San Diego, USA, and PhD in Electrical Engineering from IIT Delhi. Dr. Grover worked with STMicroelectronics for over 18 years and has led large teams on multi-million dollar projects. He presently teaches at IIIT Delhi as an Associate Professor. He leads the VLSI Circuits and Systems (ViCAS) lab at IIIT Delhi and has numerous publications and patents.
His research interests include Memory Design, Digital Circuits and System Design, Safety and Security in hardware, and inventive problem solving methods.

Prof. Sudhanshu S. Jamuar pursued PhD degree from IIT Kanpur (1977).
He is presently Visiting Professor at IIIT Delhi. In his more than 45 years long teaching career, he has also taught at other prestigious institutes like IIT Delhi, IIT Dhanbad, and Universiti Malaya (UM), Universiti Putra Malaysia (UPM) and Universiti Malaysia Perlis (UNIMAP) in Malaysia.
Prof. Jamuar's research interests include Analog and Digital circuits design, Instrumentation systems and Communication systems.
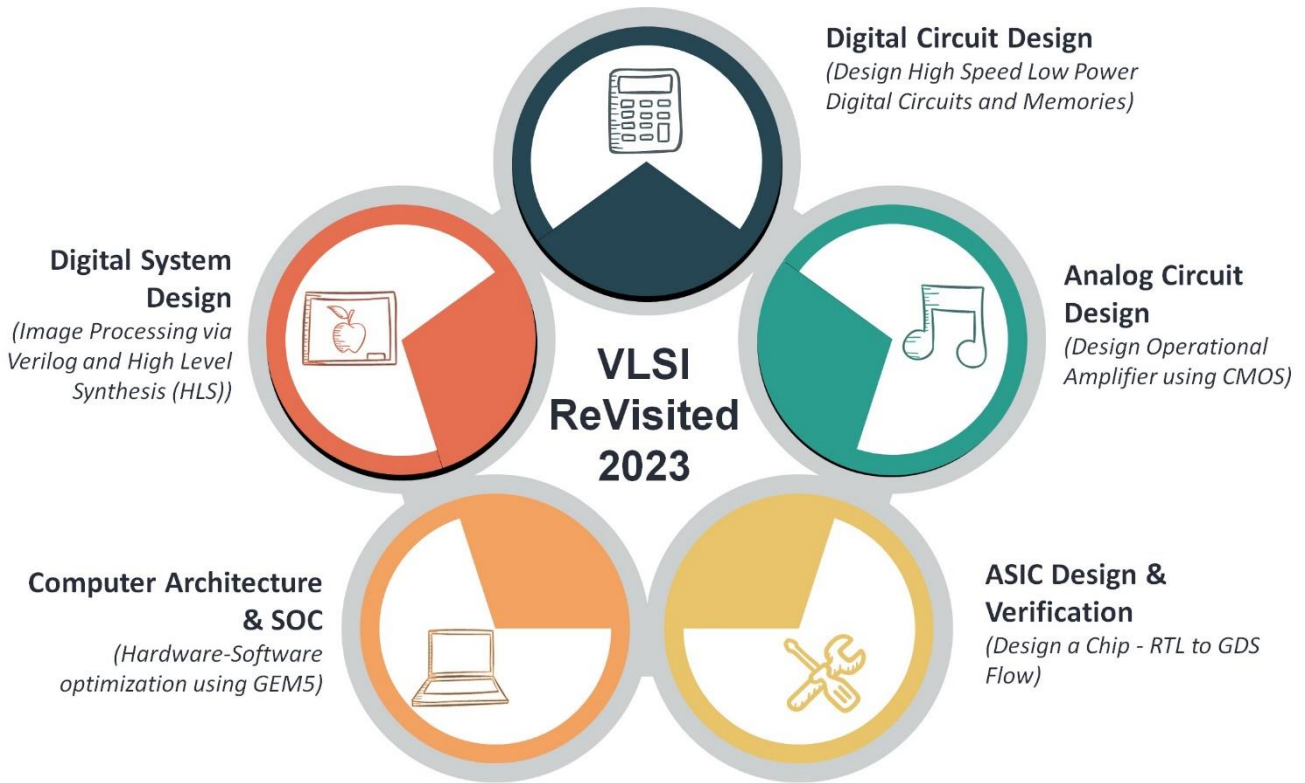

Dr. Sujay Deb received PhD from the School of Electrical Engineering and Computer Science, Washington State University, Pullman, WA (2012). He is an Associate Professor at IIITD. Earlier, he has also worked as an intern at Intel Labs, Hillsboro.
His research Interests are broadly in the areas of power and performance efficient and reliable Network-on-Chip (NoC) communication fabrics, Heterogeneous System Architectures (HSA), hardware for deep learning, low cost bio-sensors for preventive healthcare.

Dr. Sneh Saurabh obtained his PhD from IIT Delhi in the year 2012 and B.Tech. (EE) from IIT Kharagpur in the year 2000. He worked in the semiconductor industry for around sixteen years and has worked at Cadence Design Systems, Synposys India, Magma Design Automation, and Atrenta India.
He is interested in Nanoelectronics, Exploratory Electronic Devices, Energy-Efficient Systems, and VLSI Design and Verification and CAD for VLSI.

Dr. Sumit J. Darak received an Engineering degree from Pune University, India, and PhD from NTU, Singapore, in 2007 and 2013, respectively. He is an Associate Professor with IIIT-Delhi, and SoC Consultant with Apexplus Technologies, Hyderabad, India. His current research interests include the design of efficient algorithms for wireless, radar, and artificial intelligence (AI) applications and mapping to reconfigurable and intelligent architectures on SoC. His students have received numerous awards, such as DST Inspire Faculty Award, Second Best Paper Award at IEEE DASC 2017, Best Demo CROWNCOM 2016, Second Best Poster at COMSNETs 2019, Design Contest in VLSID 2022 and 2023, NI academic research grants and Qualcomm Innovation Fellowship 2023.

Workshop Contents

Subject	Faculty	Content	Tools/ Languages Used in Labs
Digital Circuit Design	Prof. Anuj Grover	• Introduction to VLSI Technology • Logic Design Styles – PTL, Static and Dynamic • Sequential Circuits • Memory Cell and Periphery Circuits	• Electric/ Virtuoso • LTSpice/ Eldo
Analog Circuit Design	Prof. S. S. Jamuar	• Basics of MOS Transistors • Basic Amplifier and Frequency Response • Current Mirrors • Differential Amplifiers • Operational Amplifiers	• Electric/ Virtuoso • LTSpice/ Spectre
Computer Architecture & SoC	Prof. Sujay Deb	• Introduction to Computer Architecture • In-depth study of pipelining and hazards • Superscalar architectures • Processor Memory sub-system • Multi-core SoCs and Research Directions	• Gem5
ASIC Design & Verification	Prof. Sneh Saurabh	• Overview of ASIC Design Flow • Logic Synthesis • Static Timing Analysis • Formal Verification • Physical Design	• Yosys • OpenSTA • Openroad
Digital System Design	Prof. Sumit J Darak	• Finite State Machine • AXI Protocol • Image Processing (Image Filtering) • High Level Synthesis (HLS) • Image Processing via HLS	• C++ to Verilog via HLS

VLSI REVISITED SCHEDULE

JULY 2023

SUN	MON	TUE	WED	THU	FRI	SAT
30	31					1
2	3 DCD	4 DSD (Verilog)	5 CA	6 DSD (Verilog)	7 CA	8
9	10 ADV	11 CA	12 ADV	13 CA	14 ADV	15
16	17 ADV	18 ACD	19 DCD	20 ACD	21 DCD	22
23	24 DCD	25 ACD	26 DSD (HLS)	27 ACD	28 DSD (HLS)	29

*DCD - Digital Circuit Design
*DSD - Digital System Design
*ACD - Analog Circuit Design

*ADV - ASIC Design and Verification
*CA - Computer Architecture and SOC

Methodology

Daily
- 3-hr live lectures
  - 10 am – 1 pm for DCD, DSD, ADV, CA
  - 2 pm – 5 pm for ACD
- 2-hr lab sessions (6pm – 8pm IST)
- Short take-home quiz to reinforce the most important concepts taught in the day

Additionally
- Assignments to supplement lectures with hands-on experiments on EDA tools
- Sessions by Industry Leaders from top VLSI and EDA companies
- Summative quiz to assess learning
- Regular feedback to continuously improve sessions
- Interaction with Industry leaders

Complimentary*
- Quick training module on these industry standard tools like Eldo, Virtuoso, Spectre.

when tool licenses are available at your college (SMDP program)/ place of work (industry)

Key Outcomes of the Workshop

The workshop envisages to give knowledge, tools, and methods to the participants for them to
- choose design styles and design circuits to meet Power-Performance-Area (PPA) specifications
- design an operational amplifier to meet design specifications
- design a Sigma-Delta ADC
- evaluate hardware and software co-design techniques using Gem5 software
- design and implement a digital circuit from RTL to layout
- do complete end-to-end image processing from C++ to Verilog to High Level Synthesis

Who should Attend

This summer school will add significant value to:
- Faculty wishing to get exposed to VLSI EDA tool-set and modern online pedagogy
- Research scholars starting off with research in VLSI
- Industry professionals intending to refresh basic concepts to broaden their scope of contribution
- Recent graduates joining as a Circuit (and/or) System designers in a VLSI organization
- Final year B.Tech/ M.Tech students looking for making a career in VLSI either in industry or academia
- M.Tech students intending to get exposure to and choose career path in VLSI
- Pre-final year B.Tech students toying with the idea of VLSI as a career option
- This is a Refresher program. Students who haven't done similar coursework may find the sessions very fast paced. However, most 3rd year B.Tech students are able to manage well and use this summer course as glimpse of what to expect when they pursue a specialization in VLSI Design.

Why you should Attend

- To refresh concepts in VLSI Design from some of the best faculty in the country
- To get a certification from IIIT Delhi and IEEE CASS-CSS Delhi Chapter
- To get hands-on practical experience alongside theoretical knowledge
- To prepare yourself for a flourishing career in VLSI Design

Registration Rates$^{\$*}$

Registration rates per module (in INR)

	Indian Students	Indian Faculty/ International Students	Partner Industry Participant	Industry / International Participants
IEEE Member	2000	3200	6400	8000
Others^	2500	4000	8000	10000

40% Discounted Registration rates for full program (5 modules) (in INR)

IEEE Member	6000	9600	19200	24000
Others^	7500	12000	24000	30000

$ 10% Early Bird discount until June 4, 2023
* rates are inclusive of GST
^ Additional 10% discount on group registrations of 4 or more

Resources Required

Since this is an online workshop, the participants will instead be required to arrange the following during the sessions:

- A laptop/ desktop (mandatory) with
    - Online Meeting Software - Zoom Meetings/ Google Meet
    - Microphone, Speakers, and camera
- Ensure that you have access to the following toolset
    - Schematic and Layout entry tools – Virtuoso, Custom Compiler, or Electric
    - Simulators – Eldo, Spectre, HSPICE, NGSpice, or LTSpice, Gem5
    - RTL to GDS flow tools – Yosys, OpenSTA, Openroad
    - Vivado
- Self-discipline and enthusiasm to learn

Supplementary / Reference Material for further reading

- Lecture recordings will be available for 1 month after the program
- Students can refer to the following books/ online resources for additional information
    - Digital Circuit Design:
        CMOS VLSI Design: A Circuits and Systems Perspective, *edition 4*: David Harris and Neil Weste
    - Analog Circuit Design:
        Design of CMOS Analog Integrated Circuits, *edition 2*: Behzad Razavi
        Analog Integrated Circuit Design, *edition 2*: Kenneth Martin, Chan Carusone and David Johns
    - Computer Architecture & SoC:
        Computer Architecture: A Quantitative Approach, *edition 5*: John L Hennessy and David A Patterson
    - ASIC Design & Verification:
        Introduction to VLSI Design Flow: S. Saurabh
    - Digital System Design:
        FPGA Prototyping by Verilog Examples: Pong P. Chu
        Parallel Programming for FPGAs: Ryan Kastner, Janarbek Matai, Stephen Neuendorffer

Testimonials from earlier workshops

Rufyida Nissa,
M.Tech'19, JMI
The sessions were thorough and were given hands-on experience on Eagle, LTSpice, NGSpice, Verilog, and Gem5 simulator

Shubham Roy,
B.Tech'21, MAIT Delhi
I can finally feel what goes on in the industry level which u never experienced before as it was always theoretical knowledge

Prafful Chaudhary,
M.Tech'23, IIIT Bangalore
Every single person of IIITD VLSI ReVisted was literally awesome , all my doubts are cleared. I want to thank everyone for making my 5 weeks very special and for improving my skills.

Ankesh Wasnik,
M.Tech'23, IIT Delhi
According to me entire course was valuable, I was learning new concepts every day. It was Indeed a worthwhile experience that I will keep with me.

Yash Raj,
B.Tech'21, IIT Dhanbad
There was no compromise on the depth of content. We explored "how? And why?" at each point.

Soumya Singh,
Micron, Hyderabad
Teachers and coordinators are very good

More People Speak

- "Teachers also gave suggestions on how to build a good career, dos, and don'ts. Without exaggeration, I would say I had a great and enlightening experience."
- "I never thought that online classes can be made this much interesting, interactive, and useful."
- "For me, it's far better than my whole BTech till now."
- "course was really beneficial for me to get right with concepts and provided me with roadmap for further studies"
- "it was 10/10 experience"
- "The best part of all the lectures was the student-teacher interaction."
- "All the Prof and Instructor were highly helpful and with sound knowledge. Very grateful."
- "The topics followed a natural progression which helped us to relate the concepts"
- "the instructor really took time to make us understand even the basics if he thought that we didn't know it that well"

For Registration/ Sponsorship Queries

Indraprastha Institute of Information Technology Delhi (IIIT Delhi)
Okhla Industrial Estate, Phase-3,
Nr. Govindpuri Metro Station,
New Delhi – 110020
Phone - +91 11 2690 7494
Email – vlsi-revisited@iiitd.ac.in
web – https://iiitd.ac.in/vlsi_revisited2023